CLAIMS

1. A semiconductor structure formed by a method comprising:

forming a layer on a surface of a silicon substrate having a first thickness;

forming an opening having a first width through the layer;

forming a blanket dielectric layer having a second thickness on the layer and in the opening, the second thickness being less than the first thickness;

removing the blanket dielectric layer from the layer and bottom of the opening, but not from sidewalls of the opening, to form dielectric spacers on each side wall within the opening, the gap having a second width less than the first width;

depositing a gate electrode into the gap;

removing the layer and leaving the dielectric spacers on the substrate; and

forming source and drain regions adjacent the gate electrode.

2. The semiconductor structure of claim 1, further comprising, prior to forming the gate electrode in the gap, implanting ions through the gap using a tilted ion beam to produce a halo of implanted ions under at least one side of the gap.

3. The semiconductor structure of claim 1, further comprising, prior to forming the gate electrode in the gap, implanting ions through the gap using a normally incident or nearly normally incident ion beam.

4. The semiconductor structure of claim 1 wherein forming the gate electrode comprises:

pre-gate cleaning;

forming a gate dielectric on bottom of the gap;

forming a layer of conductive material on the layer and on the gate dielectric; and

chemical-mechanical polishing to remove the layer of conductive material from the layer but not from the bottom of the gap.

5. The semiconductor structure of claim 1, further comprising forming a self-aligned metal silicide contact to the gate and to the source and drain regions.

6. The semiconductor structure of claim 1, wherein the layer is a series of chemically distinct layers formed by the method comprising:

forming a layer of silicon nitride on the surface of the substrate; and

depositing an oxide layer on the silicon nitride layer, the deposited oxide layer having a thickness in a range of between 100 and 500 nanometers.

7. The semiconductor structure of claim 1, wherein forming an opening through the top one of the series of layers includes reactive ion etching the top one of the layers using an anisotropic etch that does not etch a chemically distinct layer beneath the top one of the series of layers.

8. An integrated circuit including field effect transistors formed by a method comprising:

forming a layer of silicon nitride on a substrate;

depositing an oxide layer on the silicon nitride layer, the oxide layer having a first thickness;

forming an opening having a first width through the oxide layer;

forming a blanket dielectric layer having a second thickness on the oxide layer and in the openings, the second thickness being half or less of the first thickness;

removing the blanket dielectric layer from the oxide layer and bottoms of the openings but not from sidewalls of the openings to form dielectric spacers on either side of gaps within the openings, the gaps having a second width less than the first width;

forming gates in each of the gaps;

removing the oxide layer and the silicon nitride layer but not the dielectric spacers; and

forming source and drain regions.

9. The integrated circuit of claim 8, further comprising, prior to forming gates in each of the gaps, implanting ions through the gaps using a tilted ion beam to produce a halo of implanted ions under at least one side of the gaps.

10. The integrated circuit of claim 8, further comprising, prior to forming gates in each of the gaps, implanting ions through the gaps using a normally incident or nearly normally incident ion beam.

11. The integrated circuit of claim 8 wherein forming gates comprises:

pre-gate cleaning;

forming a gate dielectric on bottoms of the gaps;

forming a layer of conductive material on the oxide layer and on the gate dielectric; and

chemical-mechanical polishing to remove the layer of conductive material from the oxide layer.

12. The integrated circuit of claim 8, further comprising forming self-aligned metal silicide contacts to the gates and to the source and drain regions.

13. The integrated circuit of claim 8, wherein forming an opening through the oxide layer includes reactive ion etching the oxide layer using an anisotropic etch that does not etch the silicon nitride layer beneath the oxide layer, where the opening has substantially vertical sidewalls.

14. A method of forming a feature having a critical dimension comprising:

forming a first layer having a first thickness;

forming an opening having vertical sidewalls separated by a width greater than the critical dimension extending through the first layer;

forming a blanket dielectric layer having a second thickness in the opening, on the first layer and on the sidewalls, the second thickness being half or less of the first thickness;

selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers on the sidewalls and to remove the blanket dielectric layer from a bottom of the opening without etching the first layer, the dielectric spacers separated by a gap having a width equal to the critical dimension;

forming a second layer in the gap and on the first layer;

removing those portions of the second layer formed on the first layer using a chemical-mechanical polish without removing portions of the second layer in the gaps; and

removing the first layer but not the dielectric spacers.

15. The method of claim 14 wherein forming a first layer comprises forming a series of chemically distinct layers on the surface of the substrate, a top one of the series of layers having the first thickness, the first thickness being five thousand Angstroms or less.

16. The method of claim 14 wherein forming a first layer comprises:

forming a thermal oxide on the substrate, the substrate formed from silicon;

forming a silicon nitride layer having a thickness of less than five hundred Angstroms on the thermal oxide; and

forming a silicon dioxide layer having the first thickness on the silicon nitride layer, the first thickness being five thousand Angstroms or less.

17. The method of claim 14 wherein forming a blanket dielectric layer comprises forming a blanket dielectric layer of silicon nitride.

18. The method of claim 14 wherein forming a blanket dielectric layer comprises forming a blanket dielectric layer of silicon nitride using LPCVD.

19. The method of claim 14, wherein the substrate comprises silicon and forming a second layer in the gap and on the first layer comprises:

pre-gate cleaning;

thermally growing a gate oxide on the substrate within the gap;

forming a channel within the gap;

forming the second layer of conductive material; and

chemical-mechanical polishing to remove the second layer from the first layer.

20. The method of claim 14 wherein forming the second layer comprises forming the second layer of polycrystalline silicon.